a clock source for supplying a first clock signal;

A1 Sub B1

a plurality of adjustable delay circuits receiving said first clock signal, each of said adjustable delay circuits providing a respective delayed first clock signal to a respective one of said plurality of output circuits, wherein each adjustable delay circuit contains a programming circuit for programming a respective delay to be applied to the respective clock signal, and wherein each programming circuit contains at least one fuse element for programming.

A3 Sub B1

15. (Amended) A processor based system comprising:

a processor; and

at least one memory circuit coupled to said processor, at least one of said processor and memory circuit including a data output apparatus comprising:

a plurality of output circuits each of which receives and outputs a respective data signal, each said output circuit operating in response to a respective applied clock signal;

a clock source for supplying a first clock signal;

a plurality of adjustable delay circuits receiving said first clock signal, each of said adjustable delay circuits providing a respective delayed first clock signal to a respective one of said plurality of output circuits, wherein each adjustable delay circuit contains a programming circuit for programming a respective delay to be applied to the respective clock signal, and wherein each programming circuit contains at least one fuse element for programming.

A3 Sub B1

24. (Amended) A processor based system as in claim 20 wherein said switch circuit comprises a plurality of switch elements respectively coupled to said plurality of delay elements, one of said switch elements being selectively enabled to apply said first clock signal to its respectively coupled delay element.

29. (Amended) A memory device comprising:

A4 Sub B1

a memory core; and

a data output apparatus coupled to said memory core and comprising:

a plurality of output circuits each of which receives and outputs a respective data signal from said core, each said output circuit operating in accordance with a respective applied clock signal;

a clock source for supplying a first clock signal;

a plurality of adjustable delay circuits receiving said first clock signal, each of said adjustable delay circuits providing a respective delayed first clock signal to a respective one of said plurality of output circuits, wherein each adjustable delay circuit contains a programming circuit for programming a respective delay to be applied to the respective clock signal, and wherein each programming circuit contains at least one fuse element for programming.

A5 Sub B1

38. (Amended) A memory device as in claim 34 wherein said switch circuit comprises a plurality of switch elements respectively coupled to said plurality of delay elements, one of said switch elements being selectively enabled to apply said first clock signal to its respectively coupled delay element.

A6 Sub B1

41. (Amended) A method of providing data output signals comprising:

receiving a plurality of data output signals at respective output circuits; and

operating said output circuits in response to respective applied clock signals to make said data output signals available at the output of said output circuits;

providing a first clock signal;

generating each said respective applied clock signal from said first clock signal, each said respective applied clock signals having a respective adjustable delay relative to said first clock signal; and

programming each respective adjustable delay by modifying a conductive state of at least one of a fuse element and an anti-fuse element to select a delay rate.

Add new claims 49-51 as follows:

49. A data output apparatus comprising:

a plurality of output circuits each of which receives and outputs a respective data signal, each said output circuit operating in response to a respective applied clock signal;

a clock source for supplying a first clock signal;

a plurality of adjustable delay circuits receiving said first clock signal, each of said adjustable delay circuits providing a respective delayed first clock signal to a respective one of said plurality of output circuits, wherein each adjustable delay circuit contains a programming circuit for programming a respective delay to be applied to the respective clock signal, and wherein each programming circuit contains at least one anti-fuse element for programming.

50. A processor based system comprising:

a processor; and

at least one memory circuit coupled to said processor, at least one of said processor and memory circuit including a data output apparatus comprising:

a plurality of output circuits each of which receives and outputs a respective data signal, each said output circuit operating in response to a respective applied clock signal;

a clock source for supplying a first clock signal;

A7 Sub B1

a plurality of adjustable delay circuits receiving said first clock signal, each of said adjustable delay circuits providing a respective delayed first clock signal to a respective one of said plurality of output circuits, wherein each adjustable delay circuit contains a programming circuit for programming a respective delay to be applied to the respective clock signal, and wherein each programming circuit contains at least one anti-fuse element for programming.

51. A memory device comprising:

a memory core; and

a data output apparatus coupled to said memory core and comprising:

a plurality of output circuits each of which receives and outputs a respective data signal from said core, each said output circuit operating in accordance with a respective applied clock signal;

a clock source for supplying a first clock signal;

a plurality of adjustable delay circuits receiving said first clock signal, each of said adjustable delay circuits providing a respective delayed first clock signal to a respective one of said plurality of output circuits, wherein each adjustable delay circuit contains a programming circuit for programming a respective delay to be applied to the respective clock signal, and wherein each programming circuit contains at least one anti-fuse element for programming.